R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Examiner Patel is thanked for withdrawing the November 16, 2005 Office Action in favor of the current Office Action.

INTERVIEW SUMMARY

In an exchange of voice messages during December 2005, Supervisor John Follansbee stated that a new or supplemental Office Action to the November 16, 2005 Office Action would be generated. In a telephone conversation on February 11, 2006, Examiner Patel informed Applicant's representative that a new Office Action with a new due date would be available shortly. The claims were not discussed. No samples were presented. No agreement was reached regarding the claims.

SUPPORT FOR THE SPECIFICATION AMENDMENTS

Support for the specification amendments (text and drawing) may be found in the specification, for example, on page 9 lines 8-12 and FIG. 2, as originally filed. Thus, no new matter has been added.

In the replacement FIG. 6, the reference numbers for the NETWORK INTERFACE block have been changed from 104/106 to 122/124

and the spaces within the signal names OUTP and INP have been removed.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 5 lines 5-9, page 5 line 20 - page 6 line 9, page 11 lines 13-17, page 12 lines 14-21, page 14 line 8 - page 15 line 7, page 18 lines 15-21, page 20 lines 3-9, page 21 lines 1-9 and FIGS. 2-6, as originally filed. Thus, no new matter has been added.

CLAIM OBJECTION UNDER 35 U.S.C. §132

The objection to claims 1, 3, 10, 18, 19 and 20 under 35 U.S.C. §132 for new matter has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Regarding claims 1, 3, 10, 18 and 19, while Applicant's representative does not necessarily agree with the Office's interpretation of the claims, the claims have been amended in order to further prosecution.

Claim 20 provides the assembly according to claim 10, further comprising **a fourth circuit** connected to a second circuit and configured process at least one of a plurality of first parameters in an incoming packet in accordance with a pointer.

Claim 20 depends from claim 10. Claim 10 provides **a first circuit** configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet; **a second circuit** configured to (i) store a plurality of pointer values for a plurality of first parameters defined by the network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values, (ii) process a particular one of the first parameters in the incoming packet in accordance with the corresponding pointer value to produce a second parameter, and (iii) present an outgoing packet containing the second parameter; and **a third circuit** configured to frame the outgoing packet to present a transmit frame to a second network.

Referring to FIGS. 2 and 3 of the application, as originally filed, a Network 1 Interface circuit 122 may be representative of the claimed first circuit, a Protocol Processing Engine circuit 126 may be representative of the claimed second circuit, a Network 2 Interface circuit 124 may be representative of the claimed third circuit and an External Peripherals **circuit 108** may be representative of the **claimed fourth circuit**. Furthermore, the text of the application, as originally filed, states:

> The interface 114 may provide a mechanism to couple to the external circuit 108 to expand the parameter processing capability when desired. (Page 8, lines 18-20)

> The protocol processing engine 126 may be coupled to the interface 114 to exchange the parameters (e.g., signal PARAM) with the external circuit 108. The external circuit 108 may be operational to provide some parameter processing. (Page 11, lines 13-17)
>
> The external circuit 108 may be implemented a one or more circuits 132N-Q. (Page 13, lines 16-17)
>
> Each peripheral block 132A-Q may be designed to perform an operation on the parameters. (Page 14, lines 8-9)

Based on the above text and figures, one of ordinary skill in the art would appear to understand that the Applicant had possession of the claimed fourth circuit at the time of filing. Therefore, claim 20 is fully compliant with 35 U.S.C. §132 and the objection should be withdrawn. If the above issue is maintained, the Examiner is respectfully requested to clarify if the issue is an objection (non-appealable) or a rejection (appealable).

OBJECTION TO THE DRAWINGS

The objection to Figures 1-6 for new matter has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Please refer to the above remarks concerning the 35 U.S.C. §132 objection for an explanation where the claim elements at issue are present in the drawings.

Applicant's representative respectfully declines the request to re-label FIG. 1 from "conventional" to "prior art". MPEP 608.02(g) does not require the use of the phrase "prior art".

OBJECTION TO THE SPECIFICATION

The objection to the title is respectfully traversed and should be withdrawn.

The current title "Programmable Protocol Processing Engine for Network Packet Devices" appears to be indicative of an invention to which the claims are directed. In particular, claim 1 provides (in part) a processing circuit (e.g., programmable protocol processing engine) configured to process at a particular one of a plurality of first parameters defined by a network protocol in an incoming packet (e.g., network packets). As such, the title appears to be indicative of the claimed invention and the objection to the title should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1, 3, 10, 18 and 19 under 35 U.S.C. §112, first paragraph, written description has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claims 3 and 4 under 35 U.S.C. §112, second paragraph, indefiniteness, has been obviated by appropriate amendment and should be withdrawn.

Regarding claims 1, 3, 10, 18 and 19, while Applicant's representative does not agree with the claim interpretations provided in the Office Action (e.g., a single pointer), the claims

have been amended in the interest of advancing the prosecution. Furthermore, MPEP §2163.III.A states:

> The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. *Wertheim*, 541 F.2d at 263, 191 USPQ at 97. In rejecting a claim, the examiner must set forth express findings of fact regarding the above analysis which support the lack of written description conclusion. These findings should:
>
> (A) Identify the claim limitation at issue and
>
> (B) Establish a prima facie case by providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed.

In contrast, the Office appears to be confusing a lack of the exact claim language in the specification with an inability of one of ordinary skill in the art understanding that Applicant had possession of the invention as claimed in view of the disclosure. Per MPEP §2163, there is no *in haec verba* requirement to use the same language in the claims as used in the specification. Furthermore, no evidence is provided why one of ordinary skill in the art would not recognize that Applicant had possession of the invention as claimed. Therefore, a *prima facie* case has not been established and the rejection should be withdrawn.

Claim 20 provides a fourth circuit connected to the second circuit and configured process a select one of the first parameters in the incoming packet in accordance with the corresponding pointer value. As noted above in the response to the 35 U.S.C. §132 rejection, claim 20 may be represented in the

specification as the External Peripherals circuit 108. Furthermore, as illustrated in FIG. 3 of the application, the External Peripherals circuit 108 contains additional Peripheral circuits 132N-Q that are similar to the peripheral circuits 132A-132M within the Processing circuit 128 (part of the Protocol Processing Engine circuit 126). Therefore, one of ordinary skill in the art would appear to understand how to use and/or make the invention. As such, claim 20 is fully compliant with 35 U.S.C. §112, first paragraph, written description, and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2 and 4-17 under 35 U.S.C. §102(e) as being anticipated by Dietz et al. '725 (hererafter Dietz) is respectfully traversed and should be withdrawn.

The Federal Circuit has stated that "[t]o anticipate, ***every element and limitation*** of the claimed invention must be found in a single prior art reference, ***arranged as in the claim.***"[1] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be **no difference** between the claimed invention

[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2] Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either ***expressly or inherently described***, in a single prior art reference."[3]

Dietz concerns a processing protocol specific information in packets specified by a protocol description language (Title).

Claim 1 provides a database circuit configured to **store** a plurality pointer values. Despite the assertion on page 39 of the Office Action, the only alleged pointers that appears to be stored in any of the alleged databases are the CAM pointers stored in the CAM. Therefore, the Office appears to be arguing that only the CAM pointers of Dietz are allegedly similar to the claimed pointer values and only the CAM of Dietz is allegedly similar to the claimed database circuit. If the above is incorrect, Applicant's representative respectfully requests that the Examiner clearly identify and explain how Dietz expressly or inherently discloses where the other alleged pointers are shown stored in the other alleged databases. The Office Action approach of listing all potential databases and all potential pointers of Dietz does not address the storage claim limitation as required by MPEP §2131.

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[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[3] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

The standard is to show that the prior art elements are arranged as in the claim, not merely that the claims elements are supposedly found somewhere in the prior art. Please limit the explanation to one or two best examples to help frame the issue.

Claim 1 further provides that the plurality pointer values **are for** a plurality of first parameters defined by a network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values. In contrast, the CAM pointers (allegedly similar to the claimed pointers) do not appear to be for any of the various elements of Dietz alleged similar to the claimed first parameters on pages 39-40 of the Office Action. Therefore, Dietz does not appear to expressly or inherently disclose that the plurality pointer values are for a plurality of first parameters defined by a network protocol as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly explain how the alleged pointer values of Dietz are supposedly for the alleged first parameters of Dietz or (ii) withdraw the rejection. The Office Action approach of listing all potential pointers and all potential first parameters of Dietz does not address the claim limitation that the pointer values are for the first parameters as required by MPEP §2131. The standard is to show that the prior art elements are arranged as in the claim, not merely that the claims elements are supposedly found somewhere in the prior art.

Claim 1 further provides that each one of the first parameters is associated with a corresponding one of the pointer values. In contrast, none of the elements of Dietz alleged similar to the claimed first parameters appear to be expressly or inherently associated with a corresponding one of the elements of Dietz alleged similar to the claimed pointer values. Therefore, Dietz does not expressly or inherently disclose a database circuit configured to store a plurality pointer values for a plurality of first parameters defined by a network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values as presently claimed. Claim 10 provides language similar to claim 1. As such, claims 1 and 10 are fully patentable over the cited reference and the rejections should be withdrawn.

Claim 1 further provides a processing circuit configured to (i) process a particular one of the first parameters in an incoming packet received by the assembly in accordance with the corresponding pointer value to produce a second parameter and (ii) present an outgoing packet from the assembly containing the second parameter. In contrast, Dietz appears to be silent regarding any circuit processing a first parameter from an incoming packet in accordance with the CAM pointers (alleged similar to the claimed pointer values). Therefore, Dietz does not expressly or inherently disclose a processing circuit configured to (i) process a particular one of the first parameters in an incoming packet

received by the assembly in accordance with the corresponding pointer value to produce a second parameter and (ii) present an outgoing packet from the assembly containing the second parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) provide one or two clear examples with explanations of how Dietz allegedly expressly or inherently discloses the claimed processing circuit, using the one or two best pointer values examples previously requested, or (ii) withdraw the rejection.

Claim 10 further provides both a second circuit and a third circuit. In contrast, the arguments on pages 42 and 44 of the Office Action cite **the same ten elements** of Dietz as expressly disclosing **both** the claimed second circuit and the claimed third circuit. Assuming, *arguendo*, that the ten elements cited on page 42 of the Office Action are similar to the claimed second circuit (for which Applicant's representative does not necessarily agree), no logical explanation exists why Dietz would duplicate the same functionality ten different times in ten different circuits. Therefore, one of ordinary skill in the art could reasonably conclude that the assumption is incorrect. Furthermore, if the ten "second circuit" elements of Dietz are also configured as the claimed third circuit, then Dietz expressly discloses a different structure than as presently claimed. In particular, the claim allocates a portion of the assembly design into two circuits

whereas Dietz allegedly allocates the same design portion into a single circuit (ten different times). Therefore, Dietz does not appear to expressly or inherently disclose both a second circuit and a third circuit as arranged in the claim. As such, claim 10 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that the database is further configured to store a plurality of offset values and a plurality of length values for the first parameters, each one of the first parameters being further associated with both a corresponding one of the offset values and a corresponding one of the length values. In contrast, Dietz appears to be silent regarding a database circuit storing all of (from claim 1) a plurality of pointer values, (from claim 2) a plurality of offset values and (from claim 2) a plurality of length values. Therefore, Dietz does not expressly or inherently disclose that the database is further configured to store a plurality of offset values and a plurality of length values for the first parameters, each one of the first parameters being further associated with both a corresponding one of the offset values and a corresponding one of the length values as presently claimed. Furthermore, the list of alleged pointers, alleged offsets and alleged lengths provided in the Office Action fails to address where Dietz expressly or inherently discloses all of the alleged pointers, alleged offsets and alleged lengths being stored

in a database circuit. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly identify one or two database circuits of Dietz that allegedly store elements similar to the claimed pointer values, similar to the claimed offset values and similar to the claimed length values and show where Dietz discloses the alleged storing in the database circuit or (ii) withdraw the rejection.

Claim 2 further provides that the processing circuit is further configured to **partition the incoming packet in accordance with** at least one of the offset values and at least one of the length values to extract the particular first parameter. In contrast, Dietz appears to be silent regarding the use of (from claim 1) a pointer value, (from claim 2) an offset value and (from claim 2) a length value to partition an incoming packet. Therefore, Dietz does not expressly of inherently disclose that the processing circuit is further configured to partition the incoming packet in accordance with at least one of the offset values and at least one of the length values to extract the particular first parameter as presently claimed. Claim 11 provides language similar to claim 2. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed processing circuit, the claimed offset value, the claimed length value and the claimed particular first parameter and explain how the identified elements of Dietz allegedly anticipate

the claim limitations or (ii) withdrawn the rejection. The Office Action approach of listing all potential processing circuits, all potential pointers, all potential offsets and all potential lengths of Dietz does not address the "partition ... in accordance with" claim limitation as required by MPEP §2131. The standard is to show that the prior art elements are arranged as in the claim, not merely that the claims elements are supposedly found somewhere in the prior art.

Claim 4 provides that the processing circuit comprises a plurality of peripheral blocks (i) coupled to a parsing circuit, (ii) identified by the pointer values and (iii) configured to perform a plurality of processes involving the first parameters. Despite the assertion on page 47 of the Office Action, Dietz does not expressly disclose that any among (i) "portions of the network monitor 300 of figure 15", (ii) "portions of the packet acquisition device 1502 of figure 15", (iii) "portions of the parser sub-system 301 of figure 15", (iv) "portions of the analyzer sub-system 303 of figure 15", (v) "portions of the RMON probe of col., 25, lines 41-57", (vi) "portions of device of data communications network 125 of figure 1", (vii) "portions of device handling extraction engine of figure 10" and (viii) "compiler and optimizer 310 of col., 8, lin 48-col., 9, line 3" include a plurality of peripheral blocks coupled to a parsing circuit. The Office Action is, at best, speculating what might by inside the various listed blocks, whereas

the standard is express or inherent disclosure. Furthermore, no inherency has been argued, let alone established. Therefore, Dietz does not expressly or inherently disclose that the processing circuit comprises a plurality of peripheral blocks (i) coupled to a parsing circuit, (ii) identified by the pointer values and (iii) configured to perform a plurality of processes involving the first parameters as presently claimed. As such, claim 4 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 provides that the database circuit is further configured to store both a second offset value and a second length value for the second parameter as defined by a second network protocol. Despite the assertion on page 48 of the Office Action, column 19, lines 1-23 of Dietz appear to be silent regarding offsets and lengths, for parameters defined by a network protocol, stored in the CAM (alleged similar to the claimed database circuit). Therefore, Dietz does not expressly or inherently disclose that the database circuit is further configured to store both a second offset value and a second length value for the second parameter as defined by a second network protocol as presently claimed. As such, claim 5 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 8 provides that peripheral blocks are configured to simultaneously processes a plurality of the first parameters.

Despite the assertion on page 49 of the Office Action, column 6, lines 1-15 of Dietz appear to be silent regarding both (i) peripheral blocks and (ii) simultaneous processing of first parameters. Therefore, Dietz does not expressly or inherently disclose or suggest that peripheral blocks are configured to simultaneously processes a plurality of the first parameters as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed peripheral blocks and show where Dietz expressly discloses that those peripheral blocks process parameters **simultaneously** or (ii) withdraw the rejection.

Claim 9 provides that the processing circuit is implemented as only hardware. Contrary to the assertion on page 49 of the Office Action, the text in column 25, lines 8-38 of Dietz discloses the presence of a state processor and an instruction database memory. One of ordinary skill in the art would consider a processor executing instructions from memory to be at least a partial software implementation. Therefore, Dietz does not expressly or inherently disclose that the processing circuit is implemented as only hardware as presently claimed. As such, claim 9 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 13 provides an interface configured to permit a selection among a plurality of frame delineation methods. Despite

the assertion on page 50 of the Office Action, none of the cited text and figures of Dietz appear to show an interface that permits selection among a plurality of frame delineation methods. Therefore, Dietz does not expressly or inherently disclose an interface configured to permit a selection among a plurality of frame delineation methods as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the interface of Dietz allegedly similar to the claimed interface and show where Dietz expressly or inherently discloses that the alleged interface permits selection among a plurality of frame delineation methods or (ii) withdrawn the rejection.

Claim 15 provides an interface configured to permit a selection among a plurality of framing methods. Despite the assertion on page 50 of the Office Action, none of the cited text and figures of Dietz appear to show an interface that permits selection among a plurality of framing methods. Therefore, Dietz does not expressly or inherently disclose an interface configured to permit a selection among a plurality of framing methods as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the interface of Dietz allegedly similar to the claimed interface and show where Dietz expressly or inherently discloses that the alleged interface permits selection among a plurality of framing methods or (ii) withdrawn the rejection.

Claim 17 provides a first circuit configured (from claim 10) to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet and (from claim 17) frame a second outgoing packet derived from a second incoming packet to present a second transmit frame to the first network. In contrast, Dietz appears to contemplate in FIG. 15 that the packet acquisition device 1502 can receive packets from a network 102, but cannot transmit frames back to the network 102. Therefore, Dietz does not appear to expressly or inherently disclose a first circuit is configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet and frame a second outgoing packet derived from a second incoming packet to present a second transmit frame to the first network as presently claimed. As such, claim 17 is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 6, 7, 12, 14 and 16 depend from claims 1 and 10 which are now believed to be allowable. Since the dependent claims contain all of the limitations of the independent claims, the dependent claims are fully patentable over the cited reference and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 3 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Official Notice is respectfully traversed and should be withdrawn.

The rejection of claim 18 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Ogawa et al. '966 (hereafter Ogawa) and Gabrick et al., U.S. Patent Publication No. 2002/0161802 (hereafter Gabrick) is respectfully traversed and should be withdrawn.

The rejection of claim 19 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Wilford et al. '247 (hereafter Wilford) and Gabrick is respectfully traversed and should be withdrawn.

The rejection of claim 20 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Yanagihara et al. '578 (hereafter Yanagihara) is respectfully traversed and should be withdrawn.

Dietz concerns a processing protocol specific information in packets specified by a protocol description language (Title). Ogawa concerns a data receiving device which enables simultaneous execution of processes of a plurality of protocol hierarchies and generates header end signals (Title). Gabrick concerns a web presentation management system (Title). Wilford concerns an architecture for high speed class of service enabled linecard

(Title). Yanagihara concerns a digital signal processor, processing method, digital signal recording/playback device and digital signal playback method (Title).

Claim 3 provides an interface through which the offset values, the length values and the pointer values are downloaded for storage in the database circuit. In contrast, none of the alleged pointers, length and offsets cited on pages 51 and 52 of the Office action appear to be stored in the CAM (alleged similar to the claimed database circuit). Therefore, Dietz and Official Notice, alone or in combination, do not appear to teach or suggest an interface through which the offset values, the length values and the pointer values are downloaded for storage in the database circuit as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly explain how Dietz allegedly teaches that the alleged pointer values, the alleged length values and the alleged offset values for the first parameters are downloaded into some database circuit through an interface or (ii) withdraw the rejection. The Office Action approach of simply listing all potential interfaces, all potential pointers, all potential offsets and all potential lengths does not address the downloading or storing claim limitations.

Claim 18 provides that the first circuit comprises a plurality of framing circuits configured to operate on a plurality of network protocols, wherein each one of the framing circuits

operates on a corresponding one of the network protocols. In contrast, all of Dietz, Ogawa and Gabrick appear to be silent regarding multiple framing circuits where each framing circuit operates on a corresponding one of a plurality of network protocols. Therefore, Dietz, Ogawa and Gabrick, alone or in combination, do not appear to teach or suggest that the first circuit comprises a plurality of framing circuits configured to operate on a plurality of network protocols, wherein each one of the framing circuits operates on a corresponding one of the network protocols as presently claimed.

Furthermore, the Office Action fails to provide appropriate evidence of motivation to combine the references. In particular, the first asserted motivation "because the framing circuits would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly" is not found in column 3, lines 44-66 of Ogawa as alleged on page 31 of the Office Action. The second asserted motivation that "a unique network protocol would support replicating and transferring information between two entities" is not credited to any reference or knowledge generally available as required by MPEP §2141.01. Furthermore, the asserted motivations do not appear to solve problems per *In re Huston*. Therefore, the asserted motivations appear to be merely conclusory statements.

Furthermore, Gabrick appears to be non-analogous art relative to Dietz and Ogawa based on the respective US classifications. Gabrick appears to have been selected only because it contains the claim phrase "unique network protocol", not because one of ordinary skill in the art would have found it to be analogous art. Therefore, *prima facie* obviousness has not been established. As such, claim 18 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 19 provides that the third circuit comprises a plurality of de-framing circuits configured to operate on a plurality of network protocols, wherein each one of the de-framing circuits operates on a corresponding one of the network protocols. In contrast, all of Dietz, Wilford and Gabrick appear to be silent regarding multiple de-framing circuits where each of operates on a corresponding one of a plurality of network protocols. Therefore, Dietz, Wilford and Gabrick, alone or in combination, do not appear to teach or suggest that the third circuit comprises a plurality of de-framing circuits configured to operate on a plurality of network protocols, wherein each one of the de-framing circuits operates on a corresponding one of the network protocols as presently claimed.

Furthermore, the Office Action fails to provide appropriate evidence of motivation to combine the references. In particular, the first asserted motivation "because the de-framing circuits would enhance the handling the information associated with

the packet, and the packet related information would help enhance the software to process information for the assembly" is not found in column 2, line 59 through column 3, line 18 of Wilford as alleged on page 32 of the Office Action. The second asserted motivation that "the unique network protocol would support replicating and transferring information between two entities" is not credited to any reference or knowledge generally available as required by MPEP §2141.01. Furthermore, the asserted motivations do not appear to solve problems per *In re Huston*. Therefore, the asserted motivations appear to be merely conclusory statements.

Furthermore, Gabrick appears to be non-analogous art relative to Dietz and Wilford based on the respective US classifications. Gabrick appears to have been selected only because it contains the claim phrase "unique network protocol", not because one of ordinary skill in the art would have found it to be analogous art. Therefore, *prima facie* obviousness has not been established. As such, claim 19 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 20 provides a fourth circuit connected to the second circuit and configured process a select one of the first parameters in the incoming packet in accordance with the corresponding pointer value. The Office Action merely states that the claimed fourth circuit is taught by Yanagihara in FIG. 10A and column 1, lines 51-66:

> This invention aims to make it possible to perform rapid decoding of video data and audio data in a receiver/demodulator if there is a program change when a DVCR of the aforesaid type continuously plays back a plurality of digital broadcast programs, and this data is then input to such a receiver/demodulator.
>
> This invention further aims to provide a digital signal recording/playback device and digital signal playback method wherein there is no break in video data and audio data when the output during speed change playback of such a DVCR is input to a receiver/demodulator and decoded.
>
> To resolve the above problems, the digital signal processor according to this invention is characterized in comprising **first means for selecting a transport stream corresponding to any channel from a transport stream** containing a plurality of multiplexed channels, **second means for separating video data** and audio data in any desired program ... (Column 1, lines 51-66)(Emphasis added)

The Office Action appears to be arguing that the first means and the second means of Yanagihara somehow teach or suggest the claimed second circuit and the claimed fourth circuit. However, nowhere in the above text, or in any other section does Yanagihara appear to mention that the a fourth circuit (asserted similar to either the first means or the second means of Yanagihara) is configured process a selected of the first parameters (not identified in Yanagihara) in the incoming packet in accordance with the corresponding pointer values (not identified in Yanagihara). Since the pointer values and first parameters are disclosed in Dietz, one of ordinary skill in the art would **not** appear to understand how Yanagihara could use the pointer values from another document (or similar intrinsic pointer values) to process and first parameters from the other document (or similar intrinsic first parameters). Therefore, Dietz and Yanagihara, alone or in combination, do not appear to teach or suggest a fourth circuit connected to a second circuit and configured process at least one of the first parameters in an incoming packet in accordance with a pointer as presently claimed.

Furthermore, the Office Action fails to provide appropriate evidence of motivation to combine the references. In particular, the asserted motivation "because the another circuit would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly" is not found in column 1, lines 51-66 or FIG. 10A of Yanagihara as alleged on page 34 of the Office Action. Furthermore, the asserted motivation does not appear to solve a problem per *In re Huston*. Therefore, the asserted motivation appears to be merely a conclusory statement. As such, claim 20 is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

INFORMATION DISCLOSURE STATEMENT

The Examiner is respectfully requested to consider, sign and return the PTO-1449 forms filed 28 August 2003. The following documents have yet to be indicated as considered:

1) Wideband Packet over SONET, by Cisco Systems

2) Virtual Sub-Container Multiplexing Method for Optical Subscriber System, by Ishii et al.

3) Signaling in IP Cell-Switching, by Faten Ben Slimane, et al.

4) Request for Comments (RFC) 1619, by W. Simpson.

5) PPP over Simple Data Link (SDL) using SONET/SDH with ATM-like Framing, by J. Carlson et al.

6) PPP Extensions Working Group INTERNET DRAFT, by N Jones et al.

7) Protocols and Architectures for IP Optical Networking, by Jon Anderson et al.

8) Internet Engineering Task Force INTERNET DRAFT, by Daniel O. Awduche et al.

Copies of the above documents and the clean PTO-1449 forms are available in the PAIR system at 9/03/2003.

OFFICE ACTION RESPONSE TO ARGUMENTS

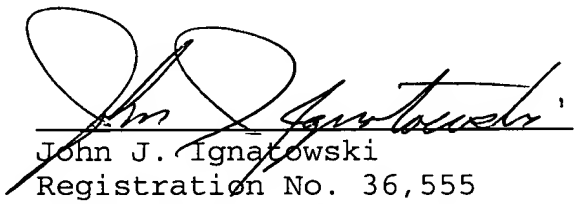
The Office is respectfully requested to refrain from attributing quotes to Applicant that were never made. In the *Response to Arguments* section of the current Office Action on pages 3-34 (and in pervious Office Actions), multiple quotes are improperly credited to the Applicant. In contrast, no such quotes exist in the amendments. If the Office wishes to paraphrase the Applicant representative's arguments, please do not use quotation marks. The use of quotation marks gives a misleading impression that Applicant's representative agrees with the Office's interpretation of the Applicant representative's own arguments.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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